

What is claimed is:

1 1. A method for fabricating trench isolations,
2 comprising:

- 3 (a) providing a substrate with a trench therein;
4 (b) forming a first dielectric layer on the
5 substrate and filling in the trench by low
6 pressure chemical vapor deposition (LPCVD);
7 (c) etching the first dielectric layer to lower its
8 surface to the opening of the trench; and
9 (d) forming a second dielectric layer on the first
10 dielectric layer and filling the trench to form
11 a trench isolation by high density plasma
12 chemical vapor deposition (HDPCVD);

1 2. The method as claimed in claim 1, wherein step
2 (a) further comprises steps of:
3 providing the substrate with a pad layer thereon;
4 defining a pattern on the pad layer;
5 etching the trench in the substrate using the
6 pattern as a mask;
7 forming an oxide liner on the bottom and sidewalls
8 of the trench by thermal oxidation; and
9 forming a nitride liner conformally on the pad layer
10 and the oxide liner.

1 3. The method as claimed in claim 2, wherein the
2 pad layer comprises a pad oxide layer and a pad nitride
3 layer overlying the pad oxide layer.

1 4. The method as claimed in claim 1, wherein the
2 aspect ratio of the trench exceeds 6.

1 5. The method as claimed in claim 1, wherein the
2 first dielectric layer is TEOS.

1 6. The method as claimed in claim 5, wherein the
2 thickness of the first dielectric layer is about
3 800~3500Å.

1 7. The method as claimed in claim 1, wherein the
2 etching is performed by anisotropic etching and wet
3 etching using hydrogen fluoride in order.

1 8. The method as claimed in claim 1, wherein the
2 first dielectric layer is lowered about 100~1000Å, by
3 etching, to the opening of the trench.

1 9. The method as claimed in claim 1, wherein
2 HDPCVD is performed with a relatively low
3 deposition/sputtering ratio and a relatively high
4 deposition/sputtering ratio in order.

1 10. The method as claimed in claim 1, wherein the
2 second dielectric layer is a silicon dioxide layer.

1 11. The method as claimed in claim 1, wherein the
2 thickness of the second dielectric layer is about
3 2500~10000Å.

1 12. The method as claimed in claim 1, further
2 comprising, after HDPCVD, planarizing the dielectric
3 layer and the pad layer.

1 13. The method as claimed in claim 12, wherein the
2 planarizing is performed by CMP.

1 14. The method as claimed in claim 13, wherein
2 the CMP includes slurry-based CMP or fixed abrasive CMP.

1 15. The method as claimed in claim 13, further
2 comprising, after CMP, performing a rapid thermal
3 annealing procedure.

1 16. A method for fabricating trench isolations,
2 comprising:

- 3 (a) providing a substrate with a first trench with a
4 relatively high aspect ratio and a second
5 trench with a relatively low aspect ratio
6 therein;
7 (b) forming a first dielectric layer on the
8 substrate and filling the trench by LPCVD;
9 (c) lowering the surface of the first dielectric
10 layer to the openings of the both trenches by
11 etching, wherein the first dielectric layer
12 forms a spacer on the sidewalls of the second
13 trench; and
14 (d) forming a second dielectric layer on the first
15 dielectric layer and filling both trenches to
16 form trench isolations by HDPCVD;

1 17. The method as claimed in claim 16, wherein step
2 (a) further comprises steps of:
3 providing the substrate with a pad layer thereon;
4 defining a pattern on the pad layer;

5 etching a first trench with a relatively high aspect
6 ratio and a second trench with a relatively low
7 aspect ratio in the substrate using the pattern
8 as a mask;
9 forming an oxide liner on the bottom and sidewalls
10 of both trenches by thermal oxidation; and
11 forming a nitride liner conformally on the pad layer
12 and the oxide liner.

1 18. The method as claimed in claim 17, wherein the
2 pad layer comprises a pad oxide layer and the pad nitride
3 layer overlying the pad oxide layer.

1 19. The method as claimed in claim 16, wherein the
2 first dielectric layer is TEOS.

1 20. The method as claimed in claim 19, wherein the
2 thickness of the first dielectric layer is about
3 500~3500Å.

1 21. The method as claimed in claim 16, wherein the
2 etching is performed by anisotropic etching and wet
3 etching using hydrogen fluoride in order.

1 22. The method as claimed in claim 16, wherein the
2 first dielectric layer is lowered about 100~1000Å, by
3 etching, to the opening of the trench.

1 23. The method as claimed in claim 16, wherein the
2 HDPCVD is performed with a relatively low
3 deposition/sputtering ratio and a relatively high
4 deposition/sputtering ratio in order.

1 24. The method as claimed in claim 16, wherein the
2 second dielectric layer is a silicon dioxide layer.

1 25. The method as claimed in claim 16, wherein the
2 thickness of the second dielectric layer is about
3 2500~10000Å.

1 26. The method as claimed in claim 16, further
2 comprising, after HDPCVD, planarizing the dielectric
3 layer and the pad layer.

1 27. The method as claimed in claim 26, wherein the
2 planarizing is performed by CMP.

1 28. The method as claimed in claim 27, wherein
2 the CMP includes slurry-based CMP or fixed abrasive CMP.

1 29. The method as claimed in claim 27, further
2 comprising, after CMP, performing a rapid thermal
3 annealing procedure.